# CIR-W4DUSS2108G Art. No. 150819

DDR4 WIDE TEMP. DIMM 2133MHz 8GB

## Description

CIR-W4DUSS2108G is a CMOS Double Data Rate IV (DDR4) Synchronous DRAM module, in Fine Ball Grid Array(FBGA) packages on a 288pin glass-epoxy substrate.

DDR4 unbuffered UDIMM series offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

## Specifications

| | |
|---|---|
| Density | 8GB |
| Pin Count | 288pin |
| Type | Unbuffered |
| Dimensions | 133.35mm x 31.25mm |
| ECC | Non-ECC |
| Component Config | 512M x 8 bit |
| Data Rate | 2133 MHz |
| CAS Latency | 15 |
| Voltage | 1.2V |
| PCB Layers | 8 |
| Operating Temp.(TCASE) | -40°C~+85°C |
| Module Ranks | Dual Rank |

## Features

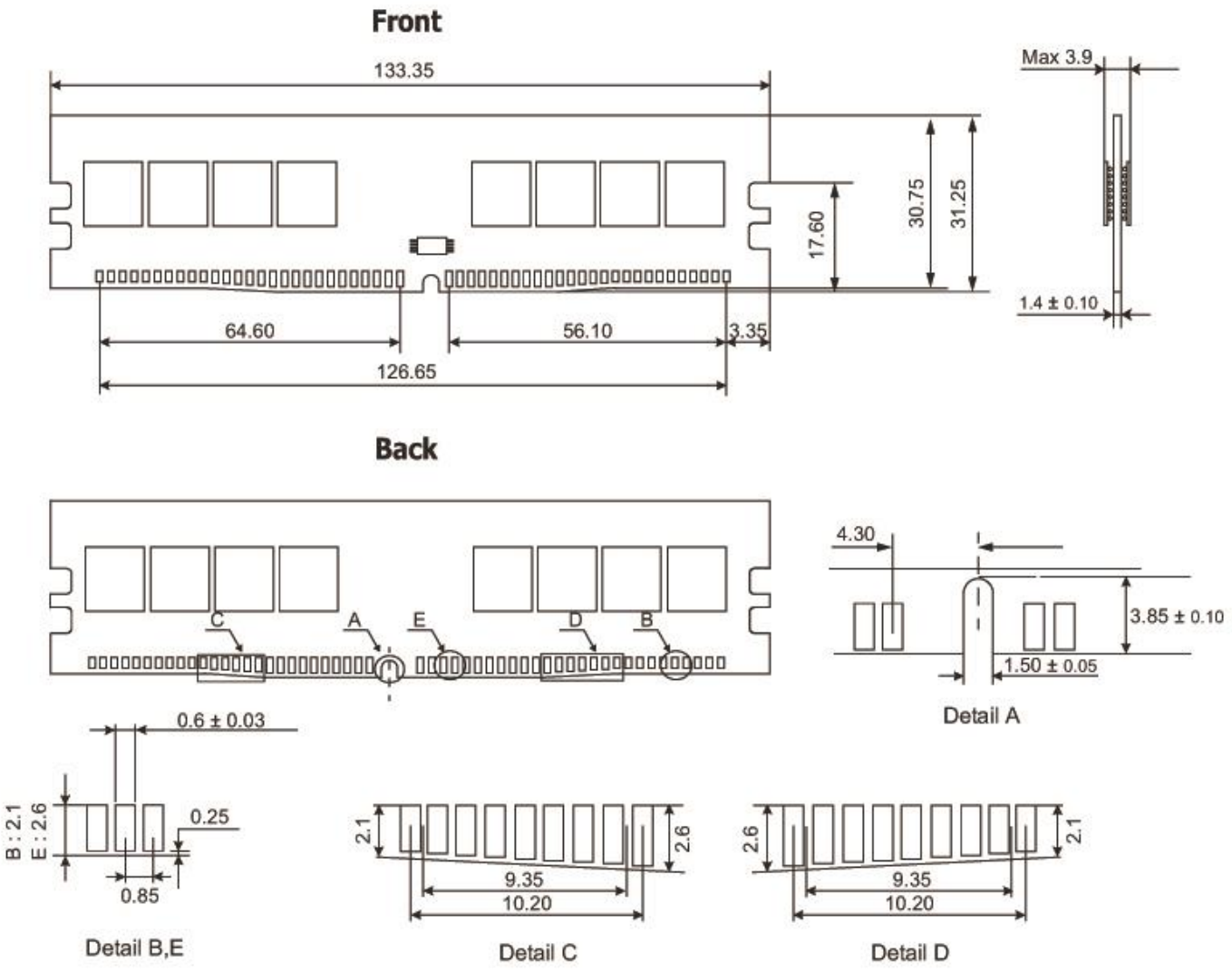
- JEDEC standard
- VDD=VDDQ = 1.2V±0.06V (1.14V~1.26V)
- Programmable CAS Latency(posted CAS): 11,12,13,14,15
- 8-bit pre-fetch
- 16 Banks (4 Bank Groups)
- Internal(self) calibration : Internal self calibration through ZQ pin
- On Die Termination using ODT pin
- Average Refresh Period
  - 7.8us ( TCASE ≤ 85˚C )
- Asynchronous Reset pin supported
- Burst Length: 8 or BC4
- POD (Pseudo Open Drain) interface for data input/output
- Serial presence detect (SPD)
- All of products are Halogen-free
- All of Lead-Free products are compliant for RoHS

## Speed Grade

| Frequency Grade | Data Transfer Rate | CAS Latency Support | | | | | CL-tRCD-tRP |
|---|---|---|---|---|---|---|---|
| | | CL11 | CL12 | CL13 | CL14 | CL15 | |
| DDR4-2133 | PC4-17000 | 1600 | 1600 | 1866 | 1866 | 2133 | 15-15-15 |

## Package Dimensions

Unit: mm




Tolerances : ± 0.15mm unless otherwise specified