

## CIR-S2DUMG8002G Art. Nr. 155127

DDR2 DIMM 800MHz 2GB

### Description

The CIR-S2DUMG8002G is 256M words X 64 bits, 2 ranks DDRII SDRAM unbuffered module, mounting 16 pieces of 1Gbits DDR2 SDRAM sealed in FBGA (  $\mu$  BGA®) package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 4bits prefetch pipelined architecture. Data strobe (DQS and /DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop (DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each FBGA (  $\mu$  BGA) on the module board.

### Specifications

Density	2GB
Pin Count	240pin
Type	Unbuffered
Dimensions	133.35mm x 30.00mm
ECC	Non-ECC
Component Config	128M x 8 bit
Data Rate	800 MHz
CAS Latency	6
Voltage	1.8V
PCB Layers	6
Operating Temp.(TCASE)	0°C~+85°C
Module Ranks	Dual Rank

### Features

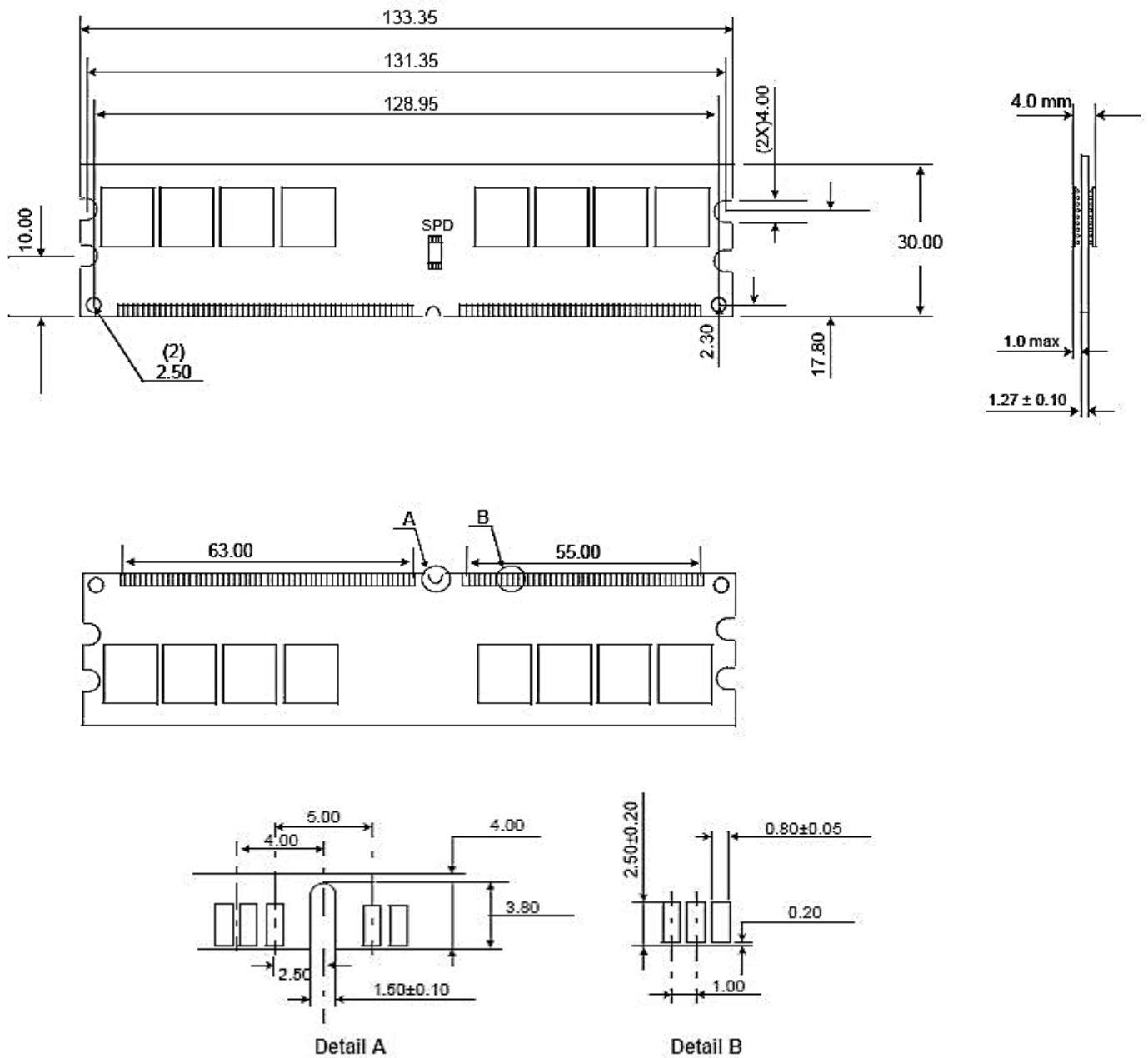
- All of Lead-Free products are compliant for ROHS
- 240-pin Dual in-line memory module(DIMM)
- 1.8V + 0.1V power supply
- 8 Banks
- JEDEC standard 1.8V I/O(SSTL\_18-compatible)
- Burst Length: 4,8
- /CAS Latency (CL):4,5,6
- Double-data-rate architecture: two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- Four-bit prefetch architecture
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- Differential data strobe(DQS,DQS#) option
- DLL to align DQ and DQS transitions with CK
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Posted CAS# additive latency (AL)
- On Die Termination (ODT)
- 64ms,8192-cycle refresh
- Serial presence detect with EEPROM
- Gold edge contacts
- Average Refresh Period  
7.8us at 0°C  $\leq$  TCASE  $\leq$  +85°C  
3.9us at 85°C  $\leq$  TCASE  $\leq$  +95°C

### Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support			CL-tRCD-tRP
		CL4	CL5	CL6	
DDR2-800	PC2-6400	533	667	800	6-6-6

### Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified