

## CIR-S2SUMG6601G Art. Nr. 155130

DDR2 SO-DIMM 667MHz 1GB

### Description

The CIR-S2SUMG6601G is 128M words x 64 bits, 1 rank DDRII SDRAM Small Outline Dual In-line Memory Module, mounting 8 pieces of 1GB bits DDRII SDRAM sealed in FBGA(  $\mu$  BGA®) package. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 4 bits prefetch-pipelined architecture. Data strobe (DQS and /DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay Locked Loop(DLL) can be set enable or disable. This module provides high density mounting without utilizing surface mount technology. Decoupling capacitors are mounted beside each FBGA(  $\mu$  BGA) on the module board.

### Specifications

Density	1GB
Pin Count	200pin
Type	Unbuffered
Dimensions	67.6mm x 30.0mm
ECC	Non-ECC
Component Config	128M x 8 bit
Data Rate	667 MHz
CAS Latency	5
Voltage	1.8V
PCB Layers	6
Operating Temp.(TCASE)	0°C~+85°C
Module Ranks	Single Rank

### Features

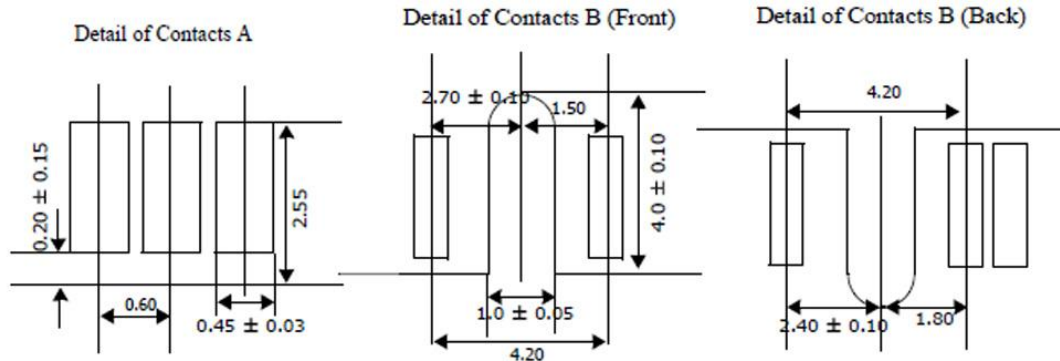
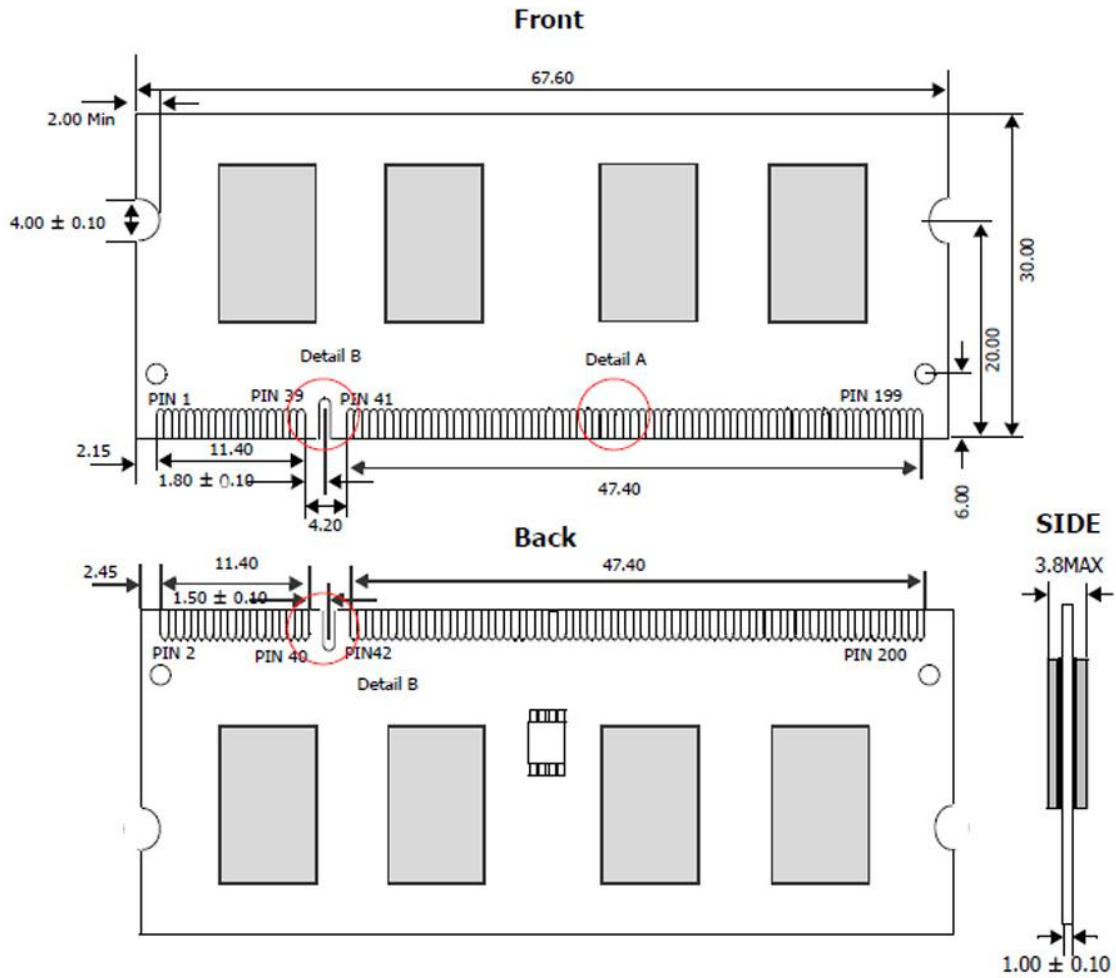
- All of Lead-Free products are compliant for ROHS
- 200-pin,small outline dual in-line memory module(SO-DIMM)
- 1.8V + 0.1V power supply
- Data rate: 667MHz(max)
- 8 Banks
- JEDEC standard 1.8V I/O(SSTL\_18-compatible)
- Burst Length: 4,8
- /CAS Latency (CL): 3,4,5
- Double-data-rate architecture: two data transfers per clock cycle
- Differential clock inputs (CK and /CK)
- Four-bit prefetch architecture
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- Differential data strobe(DQS,DQS#) option
- DLL to align DQ and DQS transitions with CK
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Posted CAS# additive latency (AL)
- On Die Termination (ODT)
- 64ms,8192-cycle refresh
- Serial presence detect with EEPROM
- Gold edge contacts
- Average Refresh Period  
7.8us at 0°C  $\leq$  TCASE  $\leq$  +85°C,  
3.9us at 85°C  $\leq$  TCASE  $\leq$  +95°C

### Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support			CL-tRCD-tRP
		CL3	CL4	CL5	
DDR2-667	PC2-5300	400	533	667	5-5-5

### Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified