CIR-S1SUMD40512 Art. N°. 162328

DDR1 SO-DIMM 400MHz 512MB

Description

The CIR-S1SUMD40512 is 64M words X 64 bits,2 Ranks Double Data Rate (DDR) SDRAM Small outline dual in-line Memory module, mounted 8 pieces of 512M bits DDR SDRAM(32Mx16) sealed in TSOPII package.

Read and write operations are performed at the cross points of the CK and the / CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode register, the on-chip Delay locked loop (DDL) can be set enable or disable.

Specifications

Density	512MB
Pin Count	200pin
Type	Unbuffered
Dimensions	67.6mm x 31.75mm
ECC	Non-ECC
Component Config	32M x 16 bit
Data Rate	400 MHz
CAS Latency	3
Voltage	2.6V
PCB Layers	6
Operating Temp.(TCASE)	0°C~+70°C
Module Ranks	Dual Rank

Features

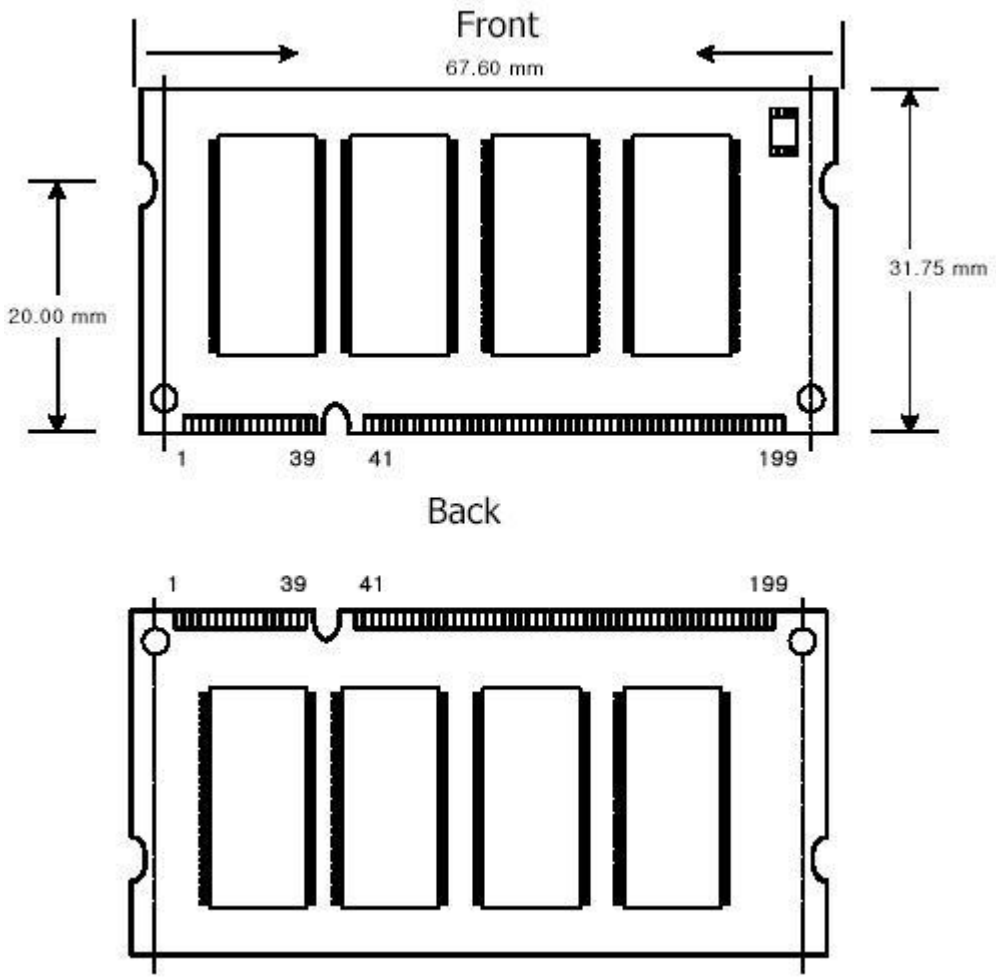
- JEDEC Standard 200-pin small outline dual in line memory module (SO-DIMM.)
- 2.6V+/-0.1V VDD and VDDQ Power supply
- Data rate: 400 MHz (max)
- SSTL-2 interface
- Double Data Rate architecture ; two data transfers per clock cycle.
- Bi-directional, data strobe (DQS) is transmitted / received with data, to be used in capturing data at the receiver.
- Data inputs, outputs and DM are Synchronized with DQS.
- DQS is edge aligned with data for READs; center aligned with data for WRITEs.
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data referenced to both edges of DQS
- Programmable burst length: 2,4,8
- Programmable /CAS latency (CL): 2.5 / 3
- Refresh cycles: (8192 refresh cycles /64ms)
- Serial Presence Detect with EEPROM
- All of Lead-Free products are compliant for RoHS

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support		CL-tRCD-tRP
		CL2.5	CL3	
DDR-400	PC-3200	266	333/400	3-3-3

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified